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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,252	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-16,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-16,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/2/04, 7/31/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This final Office action is in response to the amendment filed 7 March 2006. Claims 1-7, 9-16, 18 and 19 are pending. Claims 8 and 17 are cancelled. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 18 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As for claim 18, the application's specification and drawings only disclose a main memory and a cache (see Fig 1), not a "memory comprising a cache memory portion and a non-cache memory portion". Well known memory devices such as Uniform

Memory and Integrated Memory exhibit such properties, but the Applicant did not disclose such a device in the written description of the invention.

Appropriate correction is required.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-7, 9, 10, 11-16 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-7, 9 and 10 recite the limitations "the cache line", "the cache memory", and "the secondary memory" in the last paragraph of claim 1. There is insufficient antecedent basis for these limitations in the claim.

Claims 11-16 recites the limitations "the cache memory" in the second to last line of claim 11. There is insufficient antecedent basis for this limitation in the claim.

Claim 18 recites the limitation "the cache memory" in the last paragraph of claim 18, whereas only a "cache memory portion" is mentioned previously in the claim instead

of a "cache memory". There is insufficient antecedent basis for this limitation in the claim.

All dependent claims are rejected as having the same deficiencies as the claims they depend from. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 18 and 19 are rejected under U.S.C. 102(b) as being anticipated by Baum et al. [4,928,239].

As for claim 18, Baum et al. teaches a system, comprising:

a processor (Fig 1, Processor 19);

a memory coupled to the processor, the memory comprising a cache memory portion and a non-cache memory portion (Fig 1, combination of Cache 21 and Main Memory 13);

a stack that exists in the memory and contains stack data (Fig 4, 47; col. 5, lines 48-60);

a memory controller coupled to the memory (Fig 3, Cache Control and Replacement Control; Col 5, Lines 19-27, handling Cache Control Specifier also implies the existence of a memory controller coupled to the memory);

wherein the processor issues data requests (Fig 3, Instruction 41; Col 5, Lines 19-23); and

wherein the memory controller adjusts an allocation policy associated with the cache memory when the type of data access refers to stack data (Col 5, Lines 37-42; Col 5, Lines 48-68) that corresponds to a predetermined word (Col 5, Lines 62-63) in a cache line (Col 5, Lines 62-63; Col 4, Lines 46-50) and the cache line is not present in the cache memory (Col 5, Line 63).

As for claim 19, Baum et al. teaches a method of managing memory, comprising:

issuing a request for data (Fig 3, Instruction 41; Col 5, Lines 19-23);

indicating whether the requested data is stack data (Col 5, Lines 37-42; Col 5, Lines 48-68); and

adjusting an allocation policy associated with a cache memory when a type of data access refers to stack data (Col 5, Lines 37-42; Col 5, Lines 48-68) that corresponds to a predetermined word (Col 5, Lines 62-63) in a cache line (Col 5, Lines 62-63; Col 4, Lines 46-50) and the cache line is not present in the cache memory (Col 5, Line 63).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-7 and 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baum et al., further in view of Damron et al. [US 6,578,111 B1].

As for claims 1 and 11, Baum et al. discloses a system or a method of managing memory, comprising:

a processor (Fig 1, Processor 19);

a memory coupled to the processor (Fig 1, Cache 21 and Main Memory 13);

a stack that exists in memory and contains stack data (Fig 4, 47; Col 5, Lines 48-60);

a memory controller coupled to the memory (Fig 3, Cache Control and Replacement Control; Col 5, Lines 19-27, handling Cache Control Specifier also implies the existence of a memory controller coupled to the memory);

wherein the processor issues data requests (Fig 3, Instruction 41; Col 5, Lines 19-23); and

wherein the memory controller adjusts memory management policies based on whether the data requests refer to stack data (Col 5, Lines 28-68 – Col 6, Line 16).

Baum et al. further discloses the type of data request involves reading from the stack (Col 6, Lines 5-6), and forwarding the stack data from the secondary memory/main memory (Col 6, Lines 8-9; Col 5, Lines 9-14) to the processor, but fails to teach that adjusting the memory management policies includes not allocating the cache line containing stack data within the cache memory. However, Damron et al. discloses a similar cache memory system and method wherein cache line containing stack data (Col 4, Lines 40-45; Col 11, Lines 20-23) is not allocated (Col 9, Lines 12-14) to a cache memory (Fig 3A, Victim Cache 155) due to the access pattern and access frequency of stack data (Col 4, Lines 40-52), in order to improve cache miss rate and system operation speed (Col 9, Lines 15-20). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the applicant's invention that Baum et al.'s system and method can implement such memory management policy feature for cache lines containing stack data to improve cache miss rate and system operational speed.

As for claim 2, Baum et al. further discloses the memory comprises a first level of memory (Fig 1, Cache 21) and a second level of memory (Fig 1, Main Memory 13), and the first level of memory is faster than the second level of memory (Col 1, Lines 38-45; Col 4, Lines 20-28).

As for claim 3, Baum et al. further discloses the first level of memory comprises a cache memory (Fig 1, Cache 21) that implements a cache allocation policy, and the

cache allocation policy is adjusted based on the type of data access requested (Col 5, Lines 20-27).

As for claim 4, Baum et al. further discloses the allocation policy is adjusted when the type of data access refers to stack data (Col 5, Lines 37-42; Col 5, Lines 48-68) that corresponds to a predetermined word (Col 5, Lines 62-63) in a cache line (Col 5, Lines 62-63; Col 4, Lines 46-50) and the cache line is not present in the cache memory (Col 5, Line 63).

As for claims 5 and 6, Baum et al. further discloses the type of data request involves writing to the stack (Col 5, Lines 62-63), and adjusting the memory management policies includes allocating the cache line containing stack data within the cache memory (Col 5, Lines 63-64), and updating the stack data within the cache line without fetching data from the secondary memory (Col 5, Lines 64-68).

As for claim 7, Baum et al. further discloses the type of data request involves reading from the stack (Col 6, Lines 5-6).

As for claims 9 and 15, Baum et al. further discloses the predetermined word is the first word in the cache line (Col 5, Lines 62-63).

As for claim 12, Baum et al. further discloses the method comprises determining if the requested data corresponds to a predetermined word in a cache line in a cache memory (Col 5, Lines 20-32; Col 5, Lines 62-63).

As for claim 13, Baum et al. further discloses the method comprises determining whether the request for data is a write request or a read request (Col 5, Lines 62-63; Col 6, Lines 5-6).

As for claim 14, Baum et al. further discloses the request for data is a write request for stack data (Col 5, Lines 62-63) and the method further comprises writing data to the cache line without fetching data from a main memory (Col 5, Lines 64-68).

As for claim 16, Baum et al. further discloses enabling a valid bit associated with the cache line (Col 4, Lines 59-60).

As for claim 10, Baum et al. does not teach specifically that the predetermined word is the last word in the cache line. However, Baum et al. discloses that the predetermined word is the first word in the cache line as described above in claim 9, and the first word in the cache line is the word with the highest address (or the lowest address depending on the processor's design) in the cache line (Fig 4). It would have been obvious to one ordinarily skilled in the art at the time of the applicant's invention that the stack growth direction (which is a ordering method of storing data) is up to the

system's design decisions much like choosing between the well known byte ordering methods of Little Endian and Big Endian in a processor's design, and if the stack growth direction in Baum et al's system is reversed due to the system's design change, then the word with the highest address (or the lowest address depending on the processor's design) would become the last word in the cache line instead.

Response to Arguments

10. Applicant's arguments filed on 7 March 2006 regarding claims 1-7, 9-16, 18 and 19 have been considered but they are not persuasive. The amendment independent claims 1, 11, and the newly added independent claims 18 and 19 are mere combinations of original claims which were properly rejected in the first Office Action as they are taught by Baum et al. [4,928,239], in further view of Damron et al. [US 6,578,111 B1] as set forth above.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "... enabling data to be written to a first level of the memory without allocating data from a second level of the memory", as required by Claim 1; see Amendment, pg. 11, 2nd para., lines 2-3 and pg. 12, 1st para., lines 4-5) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from

the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In the first argument (see amendment, pg 11, 3rd para. and pg 12, 1st para.), the Applicant argues that there is no motivation to combine Baum and Damron, and that Damron does not teach the deficiency of Baum. Specifically, the Applicant argues that Damron does not teach "when the request for data is a read request for stack data reading data from a main memory without allocating a new cache line within the cache memory".

However, in the first Office Action the Examiner has indicated specifically that Baum already discloses the type of data request involves reading from the stack (Col 6, Lines 5-6), and forwarding the stack data from the secondary memory/main memory (Col 6, Lines 8-9; Col 5, Lines 9-14) to the processor, and therefore there is no need for Damron to disclose "when the request for data is a read request for stack data reading data from a main memory" as the limitation is already taught by Baum. The only deficiency in Baum is its failure to teach "adjusting the memory management policies includes not allocating the cache line containing stack data within the cache memory" during the read operation said above.

Damron et al. discloses a cache allocation method wherein read data is not allocated to a cache (Fig 3A, Victim Cache 155; col 9, lines 12-14) during a read operation involving stack data (stream data, see col. 4, lines 40-45; col. 11, lines 19-23), in order to improve cache miss rate and system operation speed (see col 9, lines 15-

20). The Examiner agrees with the Applicant's argument that the Victim Cache is related to a different cache management related issue. However, is it not the Victim Cache that is to be combined with Baum's system as argued by the Applicant, instead it is the allocation policy of not allocating cache line containing stack data into a cache memory when reading such data, that is to be combined with Baum's memory management policy. The motivation behind this combination is to avoid replacing other earlier data in Baum's cache memory that may be needed in the near future (see Damron, Abstract, and col. 4, lines 40-52; col. 9, lines 12-20). It is well known in the art that previously referenced data are stored in a cache memory according to the property of Locality of Reference, which theorizes that data which was referenced earlier might be reused again (Temporal Locality). Based on this principle, access latency can be reduced since there is a higher chance of finding the referenced data in the cache instead of fetching it from the main memory. Damron indicates that stack/stream data are accessed once and then not accessed again for a relatively long time (see col. 4, lines 40-44), and therefore the property of Locality of Reference is not utilized by placing this type of data in the cache during a read operation. In summary, if Damron's allocation policy is not incorporated into Baum's memory management policies, then access latency, cache miss rate and system operate speed are all affected negatively as previously cached data which had a higher chance of being referenced again than the stack data are now evicted from the cache and replaced by the stack data.

In the second argument (see amendment, pg 13, 1st para.), the Applicant argues that Baum does not teach "allocation policy is adjusted when the type data access refers to stack data that ... ". However, as cited in the first Office action, Baum teaches a cache line (see col. 4, lines 46-50), and the cache replacement scheme (allocation policy) is adjusted based on the type of the data, and one type of data is STACK data (see col. 5, lines 37-42) that corresponds to a predetermined word in a cache line (see col. 5, lines 62-63, reference to stack data that corresponds to the first word in a cache block) and the cache line is not present in the cache memory (if there is a cache miss, a new block must be allocated on the stack and in the cache, and there is no need to retrieve data from main memory into the cache, see col. 5, line 62-68)

In the third argument (see amendment, pg. 14, 1st para.), the Applicant argues that Baum does not teach "the requested data corresponds to a predetermined word in a cache line in a cache memory". However, the original rejection cited that Baum states "**If** the reference to the stack 47 is a STORE to the **first word in a block** and there is cache 'miss'" (see the rejection of claim 12 above), which clearly teaches the limitation in question.

In the fourth argument (see amendment, pg. 14, 3rd para.), the Applicant argues that Baum does not teach "the request for data is a write request for stack data and the method further comprises writing data to the cache line without fetching data from a main memory". However, the cited reference clearly indicates a STORE operation to

the stack, and "there is no need to retrieve data from main memory" when writing the new data to the cache line/block (see the rejection of claim 14 above, and see Baum, col. 5, lines 62-68).

In the fifth argument (see amendment, pg. 14, 5th para.), the Applicant argues that there is no teaching in Baum for "enabling a valid bit associated with the cache line". The cited reference in the previous and current rejections of claim 16 clearly stated this limitation being taught by Baum, and therefore no further explanation is given.

No new ground of rejection is presented by the Examiner in this Office Action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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13 April 2006